FIG. 1

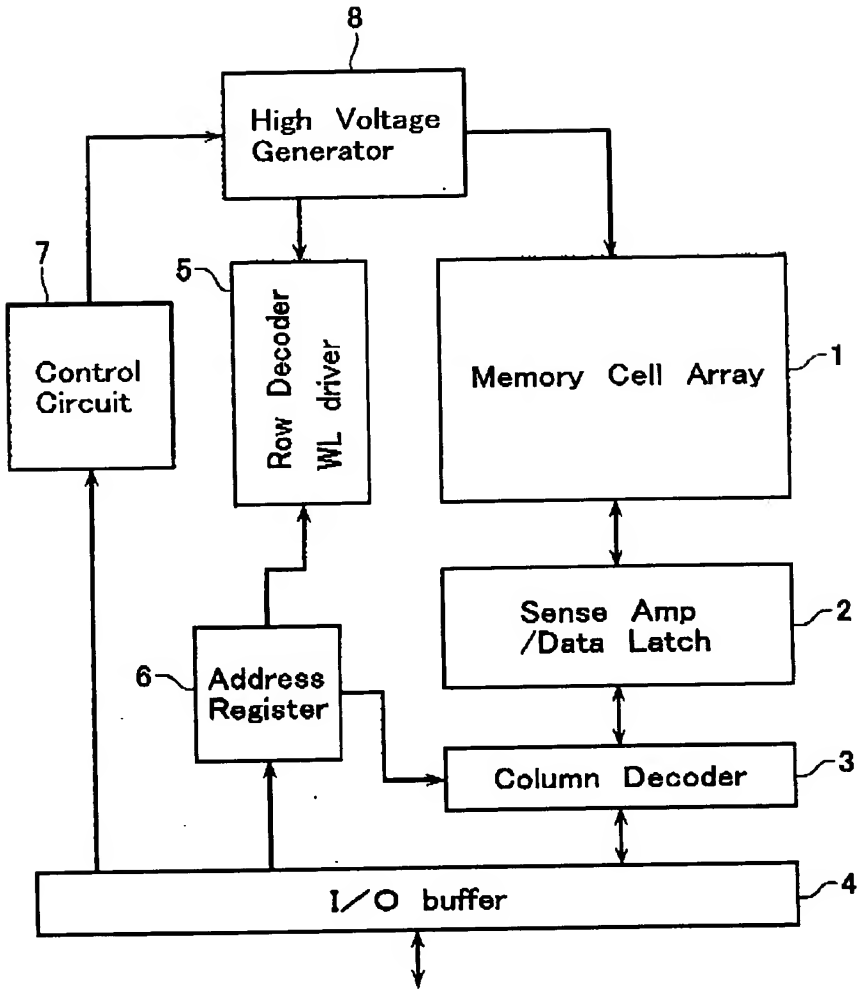

8
High Voltage Generator
7
5
Control Circuit
Row Decoder WL driver
Memory Cell Array
1
Sense Amp /Data Latch
2
6
Address Register
Column Decoder
3
I/O buffer
4

FIG. 2

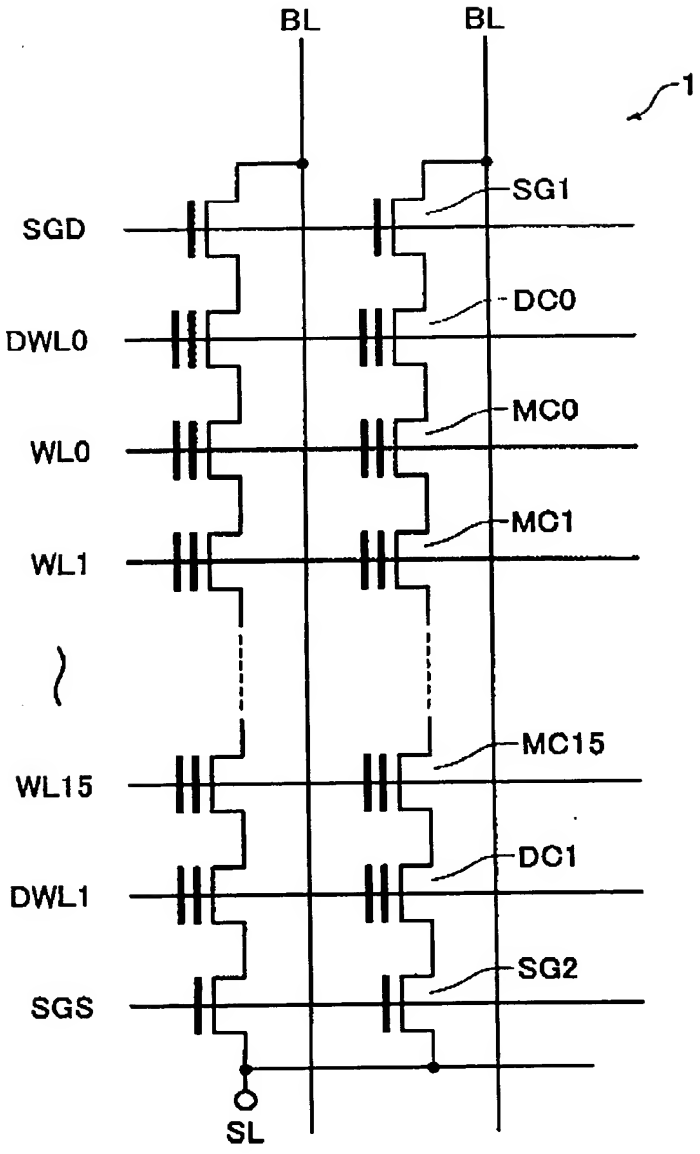

BL
BL
1
SG1
SGD
DC0
DWL0
MC0
WL0
MC1
WL1
MC15
WL15
DC1
DWL1
SG2
SGS
SL

FIG. 3

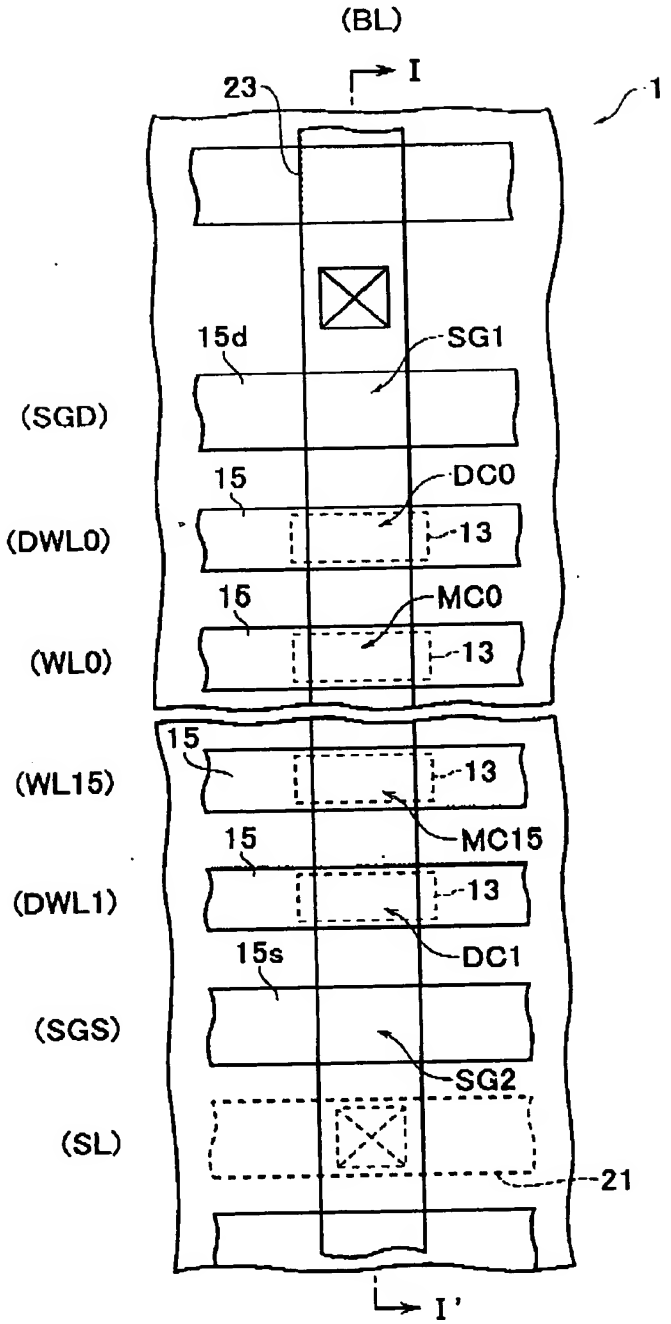

(BL)
I
23
1
15d
SG1
(SGD)
15
DC0
(DWL0)
13
15
MC0
(WL0)
13
15
(WL15)
13
MC15
15
(DWL1)
13
DC1
15s
(SGS)
SG2
(SL)
21
I'

FIG. 4

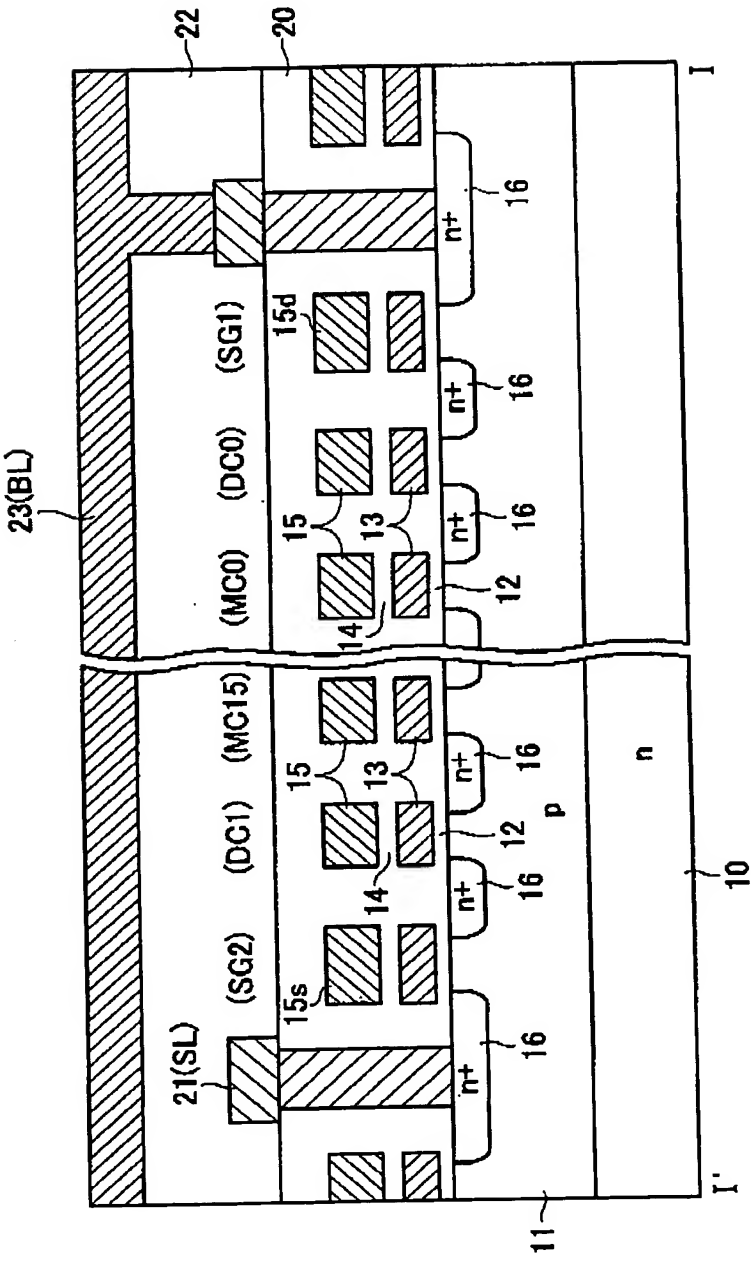

22
20
I
16
n+
15d
(SG1)
(DC0)
(MC0)
23(BL)
15
13
14
12
(MC15)
(DC1)
(SG2)
21(SL)
15s
p
n
10
I'
11

FIG. 5

	Read	Erase	Write
BL	Vbl=0.5V	Floating	"0"—Vss "1"—Vcc
SGD	Vcc	Floating	Vcc
WL	Select—Vr Non-Select—Vread	0V	Select—Vpgm Non-Select—Vpass
DWL	Vread	0V	Vpass
SGS	Vcc	Floating	0V
SL	0V	Floating	0V
P Well	0V	Vera=18V	0V

FIG. 6

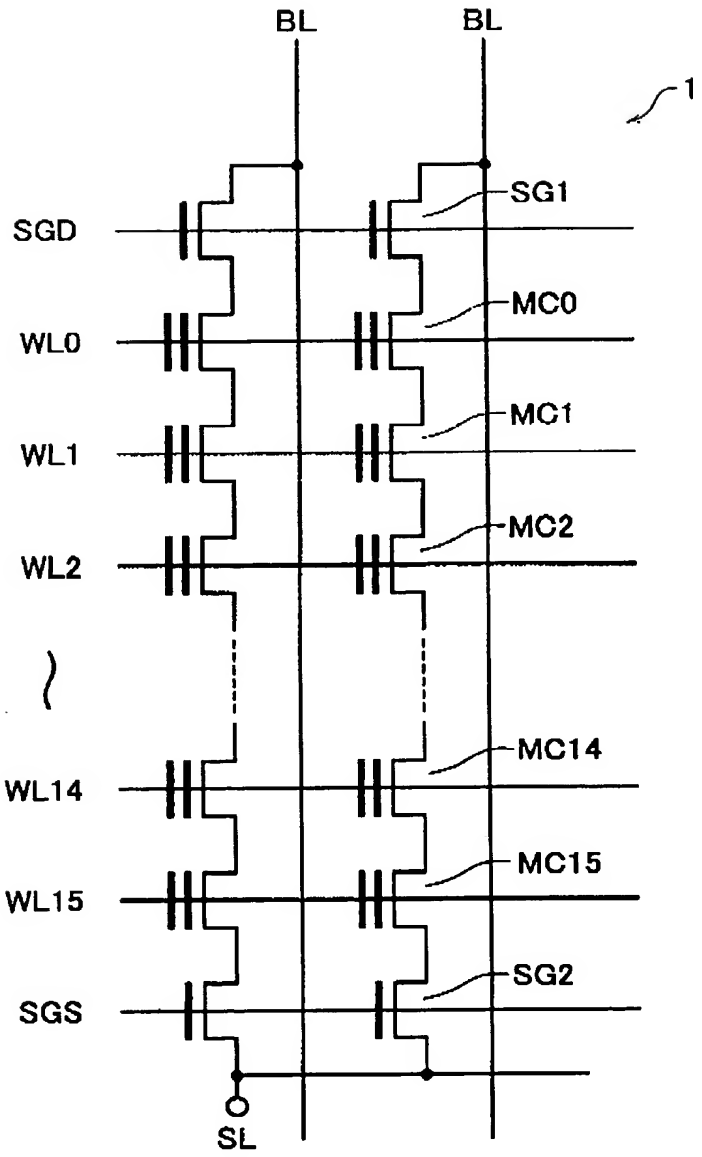

BL
BL
1
SG1
SGD
MC0
WL0
MC1
WL1
MC2
WL2
MC14
WL14
MC15
WL15
SG2
SGS
SL

FIG. 7

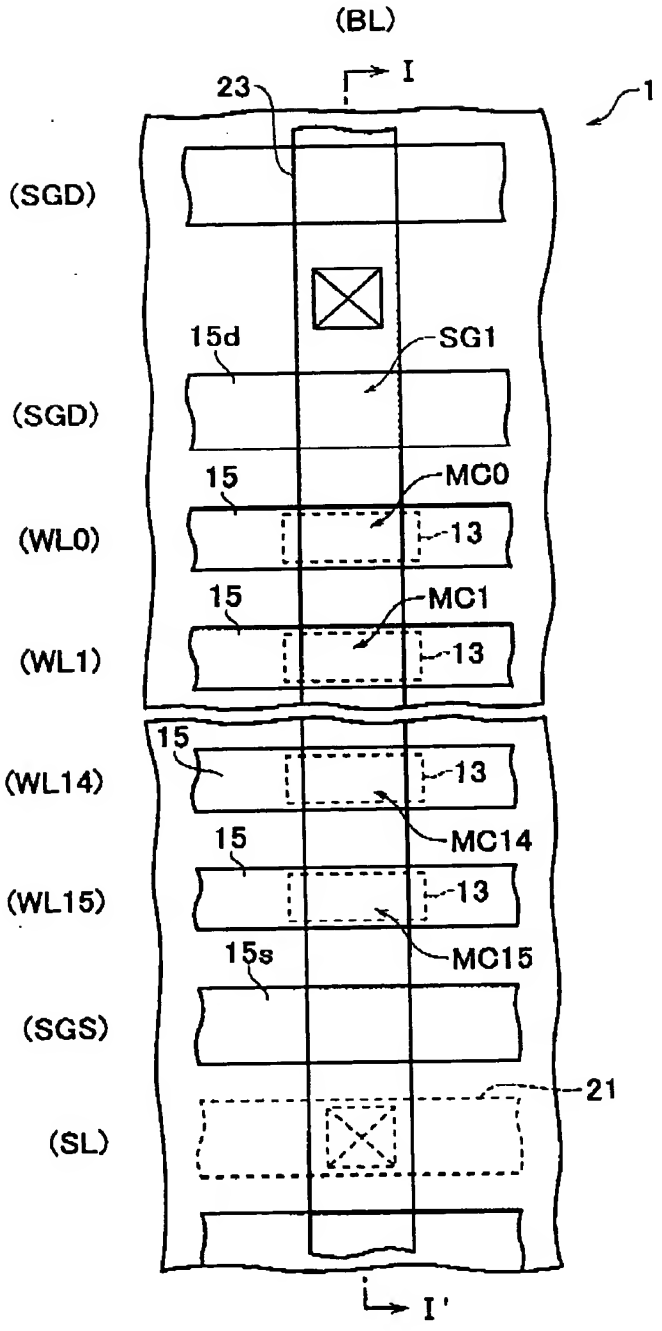

(BL)
I
23
1
(SGD)
15d
SG1
(SGD)
15
MC0
(WL0)
13
15
MC1
(WL1)
13
15
(WL14)
13
MC14
15
(WL15)
13
MC15
15s
(SGS)
21
(SL)
I'

FIG. 8

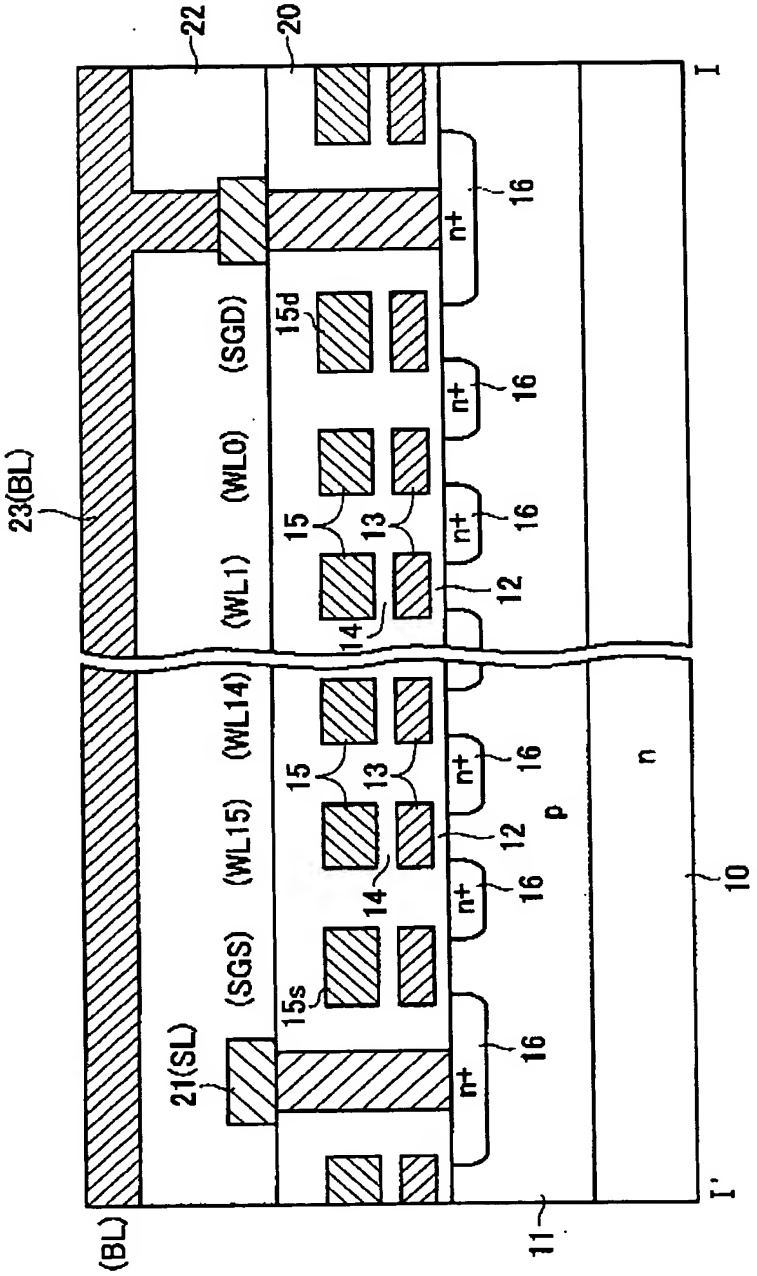

22
20
I
16
n+
15d
(SGD)
(WL0)
(WL1)
23(BL)
15
13
12
14
(WL14)
(WL15)
(SGS)
15s
21(SL)
p
n
10
11
(BL)
I'

FIG. 9

	Read	Erase	Write
BL	Vbl=0.5V	Floating	"0"—Vss "1"—Vcc
SGD	Vcc	Floating	Vcc
WL	Select—Vr Non-Select—Vread	WL0, WL15—0V WL1~WL14—0.7V	WL0, WL15 Selected Vpgm0+ΔV WL1~WL14 Selected Vpgm0
SGS	Vcc	Floating	0V
SL	0V	Floating	0V
P Well	0V	Vera=18V	0V

FIG. 10

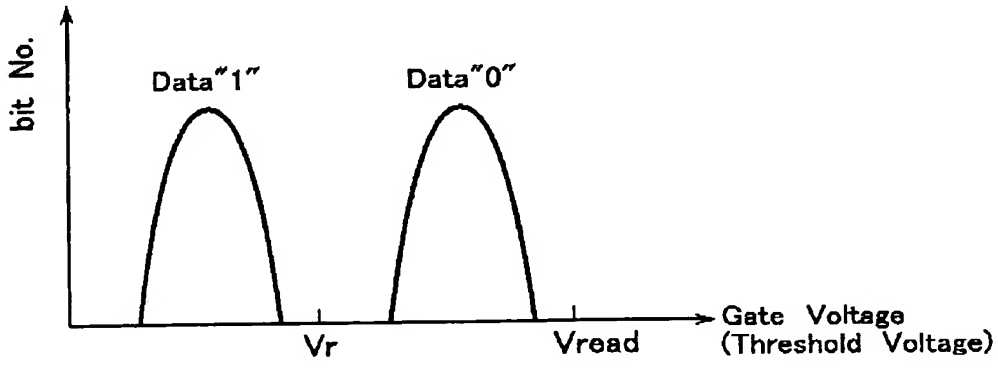


FIG. 11

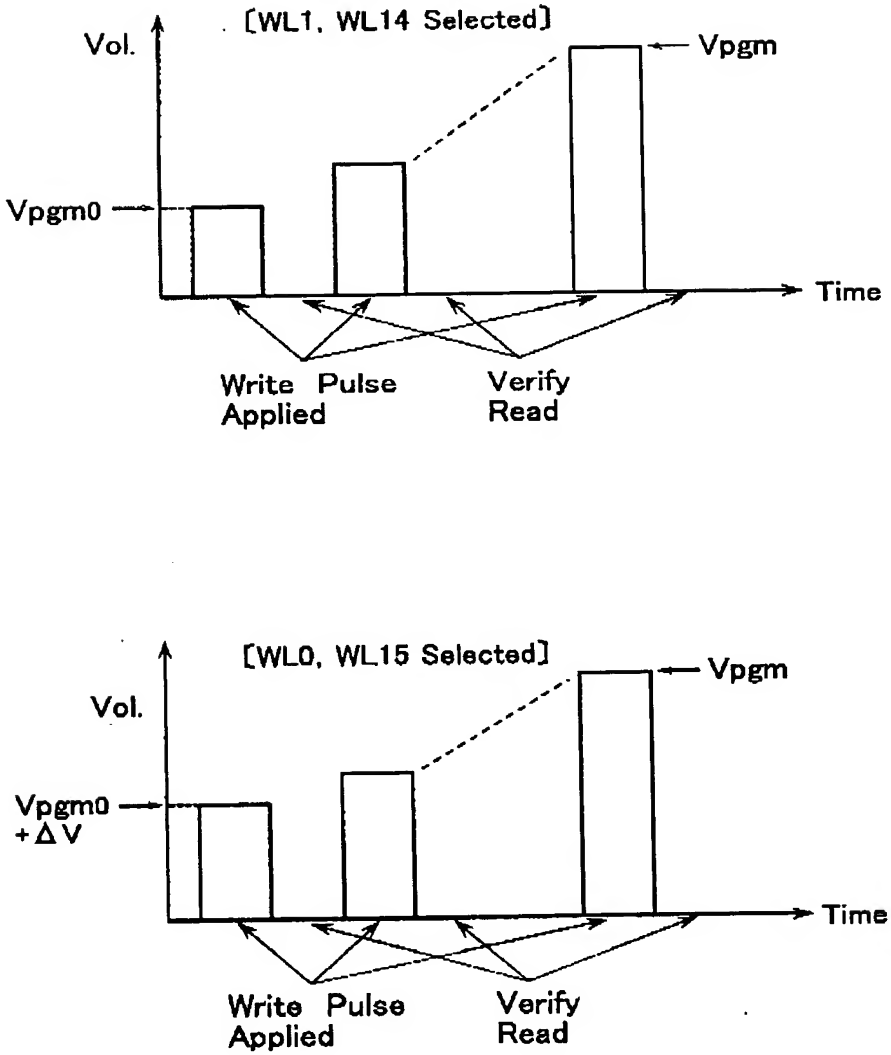

[WL1, WL14 Selected]
Vol.
Vpgm
Vpgm0
Time
Write Pulse Applied
Verify Read
[WL0, WL15 Selected]
Vol.
Vpgm
Vpgm0 +ΔV
Time
Write Pulse Applied
Verify Read

FIG. 12

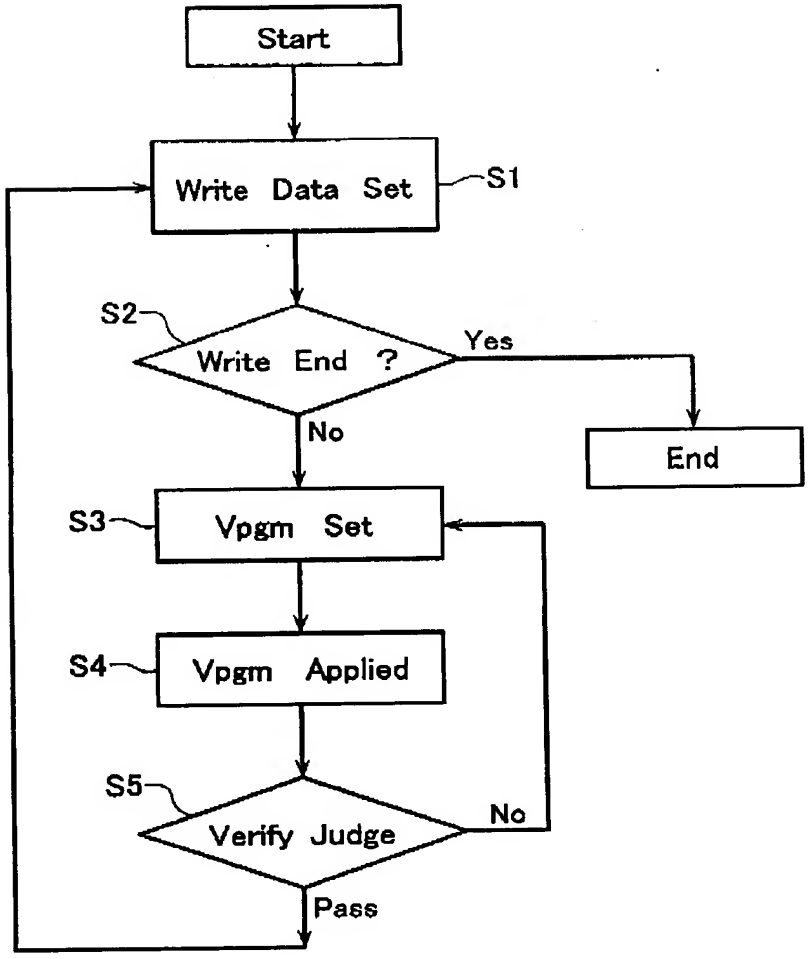

Start
Write Data Set
S1
S2
Write End ?
Yes
No
End
S3
Vpgm Set
S4
Vpgm Applied
S5
Verify Judge
No
Pass

FIG. 13

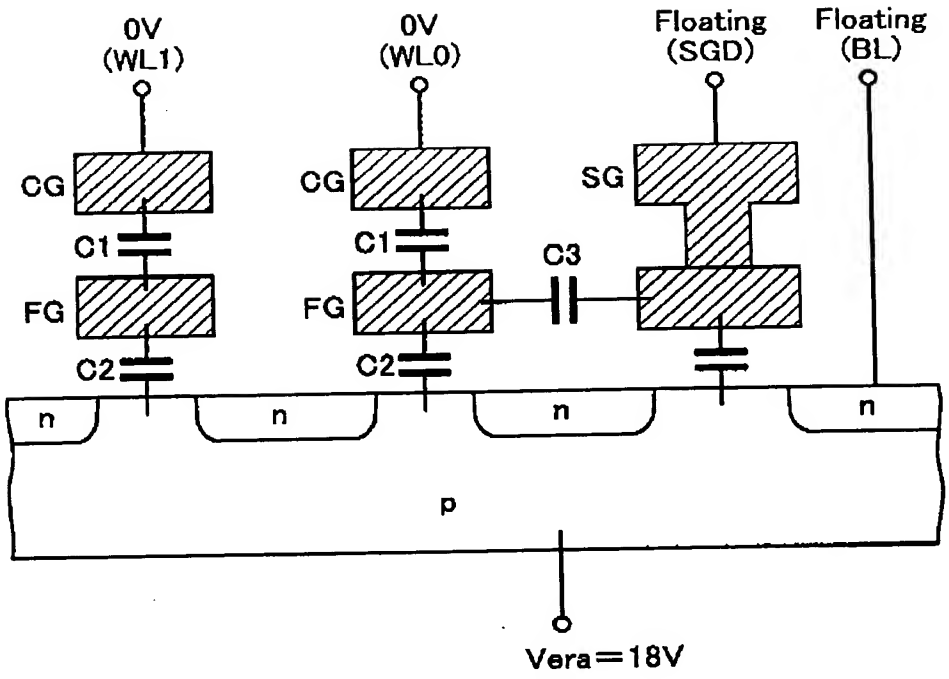

0V
(WL1)
0V
(WL0)
Floating
(SGD)
Floating
(BL)
CG
CG
SG
C1
C1
C3
FG
FG
C2
C2
n
n
n
n
p
Vera=18V

FIG. 14

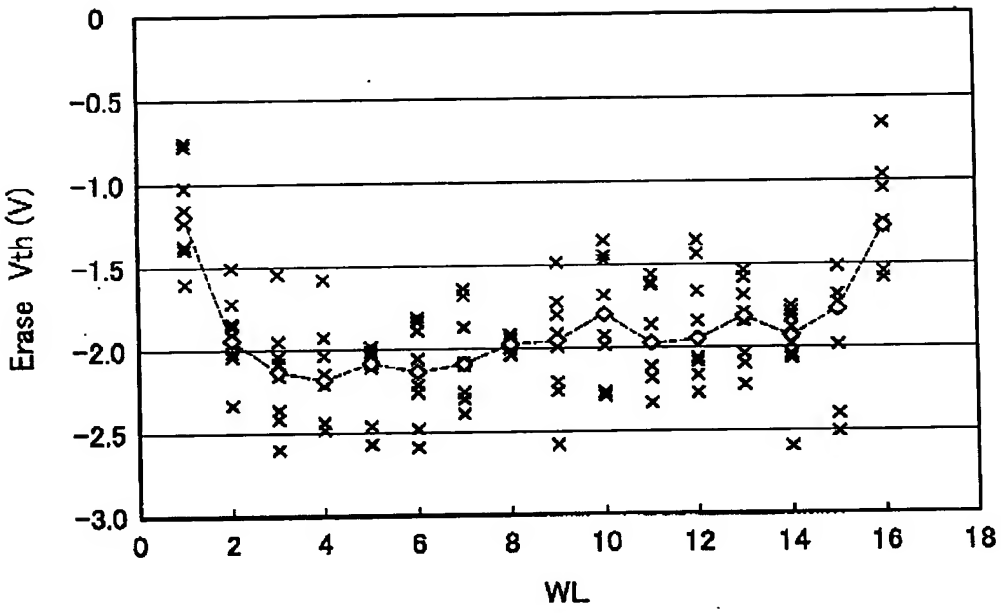
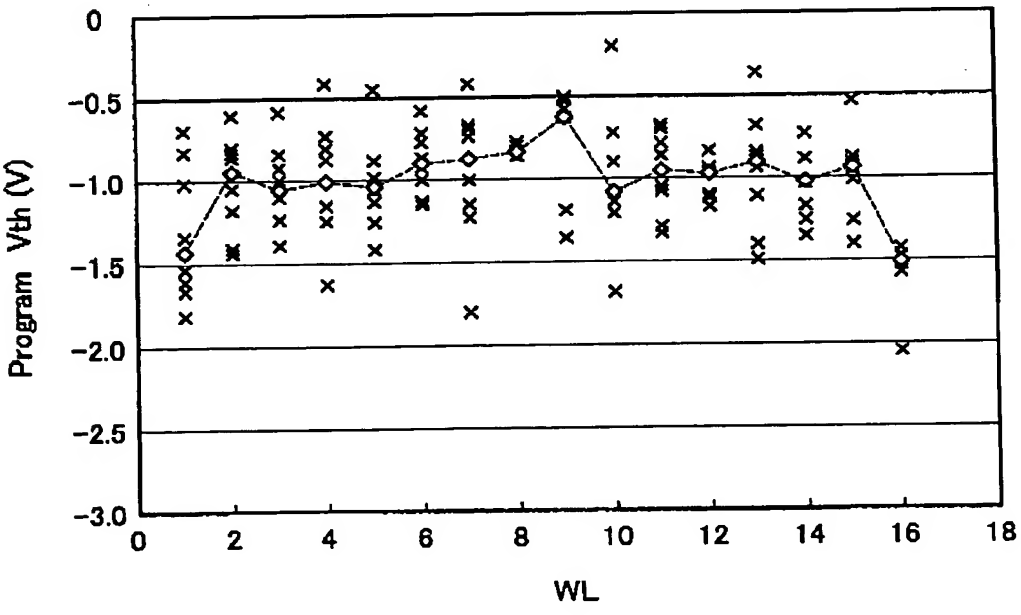

0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
Erase Vth (V)
0
2
4
6
8
10
12
14
16
18
WL

FIG. 15


0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
Program Vth (V)
0
2
4
6
8
10
12
14
16
18
WL